We claim:

1. A decoder comprising:

a SISO device that operates as a PCCC decoder in a first mode of operation and as an SCCC decoder in a second mode of operation where the device operates as per at least one trellis using an in-line addressing technique to process information.

2. The processor of claim 1 where the device processes information in accordance with an algorithm.

3. The processor of claim 2 where the algorithm is a Log MAP algorithm and the SISO device is a Log MAP processor.

4. The processor of claim 1 where in the first mode of operation the SISO device operates as a first SISO during one time period and operates as a second SISO device where the first and second SISO devices process information as per the same or different trellis.

5. The processor of claim 1 where in the second mode of operation the SISO device operates as an inner SISO during one time period whereby it processes information as per a first trellis and operates as an outer SISO during another time period whereby it processes information as per a second trellis.

6. The processor of claim 5 where the first trellis is a N_1-state Radix-K trellis and the second trellis is a N_2-state Radix-K trellis where N_1 may or may not equal to N_2 and K, N_1 and N_2 are integers equal to 1 or greater.

7. The processor of claim 1 where the SISO processor comprises:

at least one branch metric calculator;

at least one forward path metric calculator and least one backward path metric calculator where both calculators are in communication with the branch metric calculator;

at least one Log Likelihood calculator coupled to the path metric calculators; and

at least one subtractor circuit having an extrinsic information input and coupled to the at least one Log Likelihood calculator to provide at least one Log Likelihood ratio output whereby the path metric calculators and the at least one Log Likelihood calculator are constructed with Log Sum operators which are designed based on an approximation of a Jacobian definition of a Log Sum operation.

8. The processor of claim 7 in which the information is processed as per an N_1 state Radix-K first trellis and an N_2 state Radix-K second trellis when operating as an SCCC turbo decoder where N_1 is not equal to N_2 and where N_1 and N_2 are integers equal to 2 or greater and K is an integer equal to 4 or greater.

9. The processor of claim 7 where the SISO processor is operating as a PCCC decoder and N_1 may not be equal to N_2 and K is an integer equal to 4 or greater and N_1, N_2 are integers equal to 2 or greater.

10. The processor of claim 1 where the in-line addressing technique uses a block of memory for retrieving and storing values of the states of the trellis as the device processes the received information.

11. The processor of claim 1 where information is processed using a portion of the states of the trellis to perform the in-line addressing technique during a clock cycle.

12. A method of performing turbo decoding, the method comprising the step of:

processing, in accordance with an algorithm, received information as per an N-state Radix-K trellis using an in-line addressing technique where N, K are integer equal to 1 or greater.

13. The method of claim 12 where the received information is processed as per an N-state Radix-K trellis using an in-line addressing technique where N is an integer equal to 2 or greater and K is an integer equal to 4 or greater.

14. The method of claim 12 where the in-line addressing technique uses a block of memory to retrieve and store states of the trellis as information is processed per the trellis.